

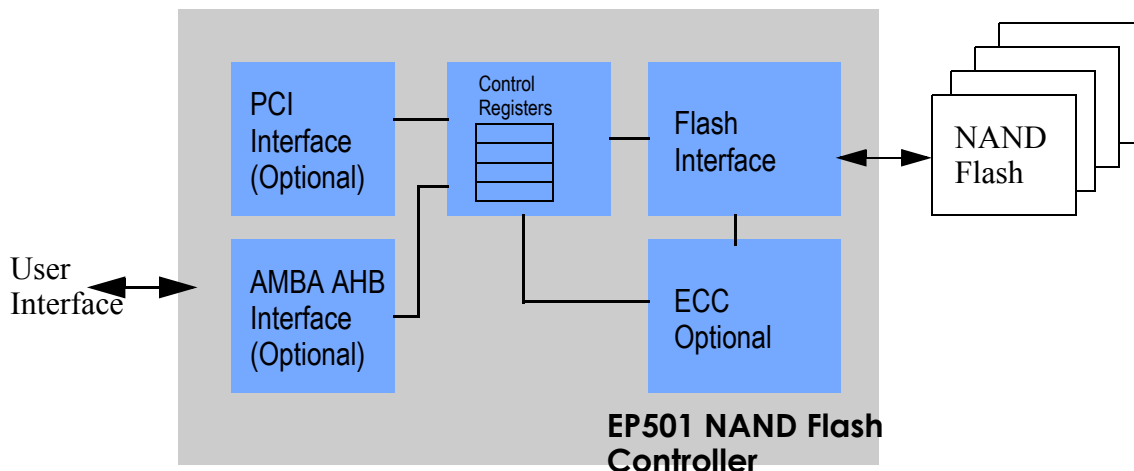


## Product Summary

### FEATURES

- Supports up to 32 Gbytes of NAND Flash devices with 8 banks.
- Each bank contains up to 5 NAND Flash connected in parallel for 32-bit data and 8-bit ECC.
- Simple user interface designed for easy on-chip integration.
- Optional AHB bus user interface.
- Programmable support for large block and small block NAND Flash devices.
- Options to provide PCI, AHB, AXI, Wishbone, SH4 and Avalon bus interface.
- Large Flash memory space can be accessed using data and index register method.
- Programmable access timing.
- User has full access to spare data in NAND Flash device.
- No wait state on reading new page by using write-triggered read.
- Support Boot ROM application by automatic page open upon reset.
- Supports two-plane page program and erase for doubling system bandwidth.
- Optional ECC protection on a per word or per page basis.
- Word-wise ECC adds 8 bits of ECC to each 32-bit word data for single-bit error correction and double bit error detection.
- Page-wise ECC provides single-bit error correction and double bit error detection for each page of data.
- Error logging with ECC correction and detection.
- Interrupt generation based on ECC error.
- Designed for ASIC and FPGA implementations.

### Block Diagram





## Description

The EP501 NAND Flash controller provides an easy interface for user to access NAND Flash devices. Typical NAND Flash devices are accessed through complicated sequence of command, address, data, and confirmation protocols. The EP501 manages all the hardware protocols and allows the user to access NAND Flash memory simply by reading and writing control registers of the EP501.

A very large size of NAND Flash memory can be accessed through a small number of control registers. The NAND Flash controller occupies only a small size in the system's memory space without sacrificing system performance. Burst access to the NAND Flash memory is supported by the controller at full memory bandwidth. Timing parameters of the controller is fully programmable so different memory speeds are supported regardless of the operating frequency of the controller.

The EP501 includes many features to improve system performance and increase system design flexibility. The Boot ROM support feature automatically open a page of the NAND Flash device upon reset. This allows the NAND Flash device to be used as the system Boot ROM. The host CPU can execute directly from the Boot ROM without programming the controller.

The Write-Trigger-Read feature allows the user to open a page of the NAND Flash device for read by writing a special code to the command register. Writing to command register takes very few cycles on the user interface, thus frees the host CPU to execute other tasks while waiting for the page to be open.

The Two-Plane program and erase procedure common found in large NAND Flash device is also supported by the controller. The two-plane operation allows two planes to be programmed or erase at the same time, thus double the data bandwidth of the NAND Flash device.

The EP501 supports optional Error Correction Code (ECC) that performs single-bit error correction and double-bit error detection. User can choose from 2 types of ECC protection: ECC for every 32-bit word or ECC for every page of data.

On word-wise ECC, 8 bits of ECC code is generated by the core for each 32-bit data. A total of 40 bit is written to the NAND Flash for each data word. Error detection and correction are automatically performed by the core with error logging through internal control registers. The core can be configure to generate interrupt on ECC error. ECC error can also be injected into the NAND Flash device if desired for diagnostic purpose. Word-wise ECC requires 32-bit NAND Flash data plus 8-bit of ECC data.

Page-wise ECC generates single bit correction and double bit detection for every 512-bytes of data. On small block NAND Flash device, one ECC code is generated for every page. On large block NAND Flash device, four ECC codes are generated for every page of data. The EP501 controller automatically generate the ECC code as each byte of data is written to the NAND Flash device. After a page of data is written to NAND Flash, the core automatically write the ECC code to the spare memory space. When data is read from the NAND Flash, the controller



core computes the expected ECC from the read data. After a page is read, the core automatically reads the stored ECC from the spare memory space and check for ECC error. If ECC error is found, the core can be programmed to generate interrupt and the error location, if correctable, is stored in its register so correction can be performed. Page-wise ECC requires 8-bit NAND Flash data path.

Several options of user interface are available for the user to choose from. The standard version features a simple user interface that is designed for on-chip system integration. It has separate address and data buses and command signals that supports burst transfer and wait state insertion. Other standard interface buses including PCI, AMBA AHB and PCMCIA (PC Card) are available. The controller acts as a target or slave device on these buses. With these standard bus interfaces, the EP501 can be integrate seamlessly with systems built on these standards.

The following are the common optional features for the NAND Flash controller.

Error Correction Code (ECC)
Different user interfaces: PCI, AHB, AXI, Wishbone, SH4, and Avalon bus.
Data width from 8 to 64 bits
More than 4 banks for memory devices.