

Wireless



Low power, high functionality, and low cost for pico/femto base stations

Boost bandwidth, keep power consumption at bay, and instantly respond to new market requirements. With Altera® Cyclone® III FPGAs, you can take control of your system specification with an unprecedented combination of low power, high functionality, and low cost for small form factor base stations, WiMAX customer premises equipment (CPE), software defined radio (SDR), and many other wireless applications.

The challenges you face

Wireless technology is evolving and standards are changing rapidly. Your next design must increase bandwidth dramatically and incorporate new standards while keeping equipment cost and power consumption as low as possible. ASICs are notoriously risky when standards and market demands are changing. Digital signal processing (DSP) devices often carry a large thermal tax, or limit the number of channels you can support. You need a low-power, low-cost solution that delivers design flexibility with low risk.

Low-power, low-cost flexibility

Because of their reprogrammability, low power, high functionality, and low cost, Cyclone III FPGAs enable a new class of wireless designs. Abundant 18x18 multipliers and on-chip memory allow you to implement low-power signal processing functions in a smaller footprint than ever before. Cyclone III FPGAs reduce cost, power, and risk for RF and channel cards in micro, pico, and femto base stations, remote radio heads, WiMAX CPE, and SDR applications, among many others. Intellectual property (IP) and tools from Altera and its wireless technology partners allow you to use pre-optimized software to save time and resources.

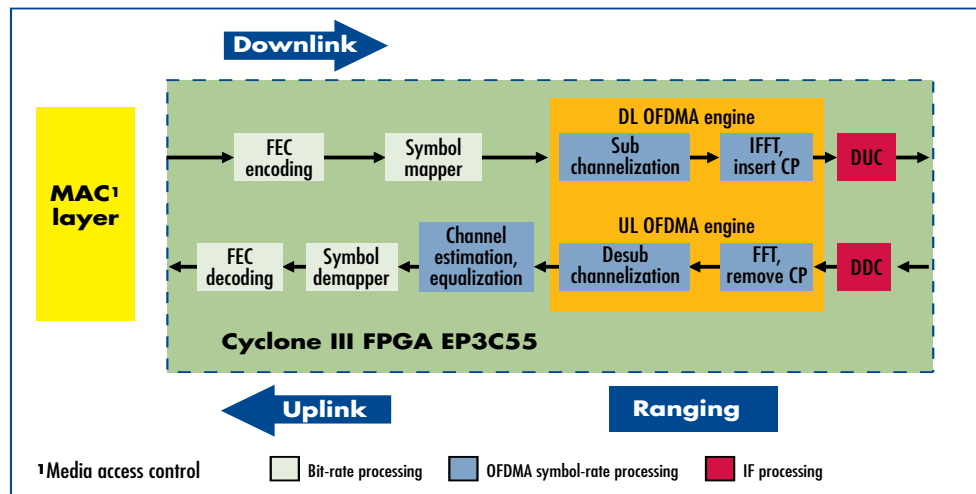
Cyclone III FPGAs for software defined radio

- Complete waveform integration for under 1 W
- Low static power for extended battery life
- 0.8-mm BGA packages (19x19 mm²) minimize board space
- Cost optimized for the best value

Cyclone III FPGA highlights

Highlighted Features	Benefits
Embedded memory	Up to 4 Mbit of on-chip memory architected for memory-intensive algorithms such as forward error correction (FEC)
DSP multipliers	Up to 288 embedded multipliers at 260-MHz performance to implement DSP-intensive functions such as finite impulse response (FIR) or fast Fourier transform (FFT)
Low power	TSMC's 65-nm low-power (LP) process technology Power optimization features in the Quartus® II design software Fifty percent lower power than Cyclone II FPGAs to meet system thermal requirements
Autocalibrating external memory interfaces	Easy implementation to support high performance of up to 400 Mbps with easy timing closure for DDR and DDR2

WiMAX pico base station



Altera enables complete low-cost wireless solutions

- Cyclone III FPGAs—optimized for wireless applications
- Application-specific reference designs
- Altera and partner intellectual property (IP) cores, including FEC, FFT/IFFT, FIR, numerically controlled oscillator (NCO), and CIC functions, among others
- White papers, including *Using Cyclone III FPGAs for Emerging Wireless Applications*
- DSP Builder—automatically integrates Quartus II software and The MathWorks MATLAB and Simulink tool
- Nios® II soft-core embedded processor
- Free Quartus II Web Edition software
- Low-cost development kits

In this WiMAX pico base station design, the digital upconverter (DUC) and digital downconverter (DDC) use complex filter architectures including FIR and cascaded integrator-comb (CIC) filters. The downlink (DL) orthogonal frequency-division multiple access (OFDMA) symbol-rate processing includes the subchannelization, inverse fast Fourier transform (IFFT), and cyclic prefix (CP) insertion functions. The uplink (UL) OFDMA symbol-rate processing includes CP removal, FFT, desubchannelization, and channel estimation and equalization functions. The following table illustrates resource usage for a WiMAX pico base station design implemented in a mid-range Cyclone III device.

The complete IF, OFDMA symbol-rate, and bit-rate processing can be implemented in a mid-range Cyclone III EP3C55 FPGA with under 2.5 W of power consumption. The abundant on-chip memory and high-speed multipliers in Cyclone III FPGAs provide a low-power, low-cost platform for implementing 3G and WiMAX base station functionality.

Picocell base station processing block utilization

		Logic elements (LEs)	Number of M9K memory blocks	18x18 multipliers	Power utilization (W)
IF processing	DUC	2,704	50	30	0.4
	DDC	4,786	46	25	0.4
OFDMA symbol-rate processing	DL OFDMA engine	4,176	33	4	0.25
	UL OFDMA engine	3,834	57	4	0.25
	Channel estimation and equalization	7,400	1	4	0.33
Bit-rate processing	Symbol mapper and demapper	1,404	3	0	0.1
	FEC (encoding and decoding)	18,511	26	0	0.6
Total		42,815	216	67	2.33
EP3C55 resources used		77%	83%	43%	2.33

Design your next low-power, low-cost wireless product today.

Unlimited possibilities.

www.altera.com/cyclone3-markets

Altera Corporation

101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544-7000
www.altera.com

Altera European Headquarters

Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 94 602 000

Altera Japan Ltd.

Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.

2102 Tower 6
The Gateway, Harbour City
9 Canton Road
Tsimshatsui Kowloon
Hong Kong
Telephone: (852) 2945 7000

