

Introduction

This document provides updated information on 64-Mbit EPCS64 serial configuration devices. These configuration devices can be used to configure Stratix® II, Cyclone™ II, and Cyclone FPGAs.



This errata sheet only pertains to EPCS64 configuration devices with the 2004 date code prior to work-week 51 (devices with 451 or later in the last three digits of the date code (see [Figure 1](#)) are fixed).

Affected EPCS64 devices have the following programming issues:

- Designers must wait two seconds after device power up before executing erase bulk and write bytes operations.
- The erase sector operation is not available.

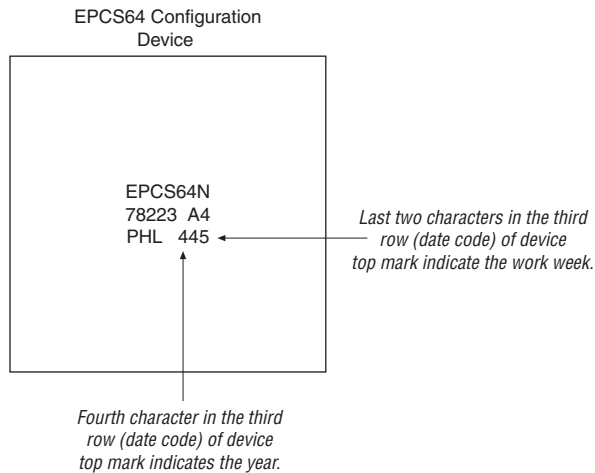
These issues do not directly impact the FPGA's Active Serial (AS) configuration process because the read bytes operation for the EPCS64 device is not affected. The read bytes operation can be performed immediately after device power up.



For more information on the erase bulk, write bytes, and erase sector operations, see the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 & EPCS64) Data Sheet* chapter in the *Configuration Handbook*.

Device Identification

All EPCS64 date codes are identified by the last three characters of the third row of the markings on the device's top side. [Figure 1](#) shows an example of the top side markings for an EPCS64 device.

Figure 1. Date Code on Device Top Mark

Programming Guidelines

Designers using a configuration device to program an FPGA can either preprogram the configuration device or write the configuration data to the configuration device after power up. Affected EPCS64 configuration devices must be powered up for at least two seconds before executing the write bytes operation.

If the EPCS64 configuration device is preprogrammed with the targeted FPGA configuration data, designers can disregard the two-second delay after power up. Designers can use any of the following methods to preprogram the EPCS64 device:

- Quartus® II Programmer
- SRunner software driver
- Serial FlashLoader in the Quartus II software
- Other customized solutions that support the EPCS64 serial interface

Fixed EPCS64 devices can perform the write bytes operation immediately without waiting two seconds after power up.

Erasing Guidelines

If the design uses a customized solution to erase and program the EPCS64 device, the designer must ensure that the configuration device does not execute the erase sector operation. The erase sector operation is not available in affected EPCS64 devices.

As a work around to erasing EPCS64 configuration devices, execute the erase bulk operation. The erase bulk operation erases the entire memory of the EPCS64 device by setting all the memory bits to the default 0xFF value. Designers should ensure that the EPCS64 device is powered up for at least two seconds before executing the erase bulk operation.



Because the erase sector operation is not available on affected EPCS64 configuration devices, the Quartus II software cannot support the remote system upgrades feature for those devices.

The erase sector operation will be available in EPCS64 configuration devices with the date code 451 or later.

References

For more information on the EPCS64 device and programming support, see the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 & EPCS64) Data Sheet* chapter in the *Configuration Handbook* on the Altera® web site (www.altera.com).

Revision History

Table 1 shows the revision history.

<i>Table 1. Revision History</i>		
Version	Date	Details of Change
1.1	March 2005	Updated date code information.
1.0	December 2004	First release of the <i>EPCS64 Configuration Device Errata Sheet</i> .



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